Program: BE Computer Engineering

Curriculum Scheme: Revised 2016

Examination: Third Year Semester V

Course Code: CSC501 and Course Name: Microprocessor

Time: 1 hour Max. Marks: 50

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| Q1. | Physical address calculated by the microprocessor in 8086 using formula |
| Option A: | Physical Address= Segment Address\*10H+Offset address |
| Option B: | Physical Address= Segment Address+10H\*Offset address |
| Option C: | Physical Address= Segment Address-10H+Offset address |
| Option D: | Physical Address= Segment Address/10H+Offset address |
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| Q2. | In 8086 microprocessor the address bus is\_\_\_\_\_\_\_ bit wide |
| Option A: | 12 |
| Option B: | 10 |
| Option C: | 16 |
| Option D: | 20 |
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| Q3. | The indexed registers are used to hold |
| Option A: | memory register |
| Option B: | offset address |
| Option C: | segment memory |
| Option D: | offset memory |
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| Q4. | 8086 has a 16 bit IO address therefore it can access\_\_\_\_\_\_IO ports |
| Option A: | 16K |
| Option B: | 32K |
| Option C: | 64K |
| Option D: | 128K |
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| Q5. | The BIU prefetch the instruction from memory and store them in |
| Option A: | stack |
| Option B: | queue |
| Option C: | register |
| Option D: | memory |
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| Q6. | the instruction, MOV AX, 0005H belongs to the address mode |
| Option A: | register |
| Option B: | direct |
| Option C: | immediate |
| Option D: | register relative |
|  |  |
| Q7. | If the data is present in a register and it is referred using the particular register, then it is |
| Option A: | direct addressing mode |
| Option B: | register addressing mode |
| Option C: | indexed addressing mode |
| Option D: | immediate addressing mode |
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| Q8. | The contents of a base register are added to the contents of index register in |
| Option A: | indexed addressing mode |
| Option B: | based indexed addressing mode |
| Option C: | relative based indexed addressing mode |
| Option D: | based indexed and relative based indexed addressing mode |
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| Q9. | The instruction perform logical AND operation |
| Option A: | AND destination |
| Option B: | AND source |
| Option C: | AND source, destination |
| Option D: | AND destination, source |
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| Q10. | To set carry flag which instruction is used |
| Option A: | STC |
| Option B: | STD |
| Option C: | SLD |
| Option D: | SCF |
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| Q11. | The IVT contain ISR address for \_\_\_\_\_\_ interrupt |
| Option A: | 128 |
| Option B: | 256 |
| Option C: | 516 |
| Option D: | 64 |
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| Q12. | Which are the user define interrupts |
| Option A: | From INT 31 to INT 255 |
| Option B: | From INT 30 to INT 255 |
| Option C: | From INT 33 to INT 255 |
| Option D: | From INT 32 to INT 255 |
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| Q13. | INT 4 occur when |
| Option A: | Breakpoint |
| Option B: | Divide by zero |
| Option C: | Overflow interrupt |
| Option D: | Single step |
|  |  |
| Q14. | In BSR mode, only port C can be used to |
| Option A: | set individual ports |
| Option B: | reset individual ports |
| Option C: | set and reset individual pins |
| Option D: | programmable I/O ports |
|  |  |
| Q15. | The strobed input/output mode is another name of |
| Option A: | mode 0 |
| Option B: | mode 1 |
| Option C: | mode 2 |
| Option D: | Mode 3 |
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| Q16. | To perform DMA transfer we need a DMA controller like |
| Option A: | 8234/3254 |
| Option B: | 8235/8255 |
| Option C: | 8236/8256 |
| Option D: | 8237/8257 |
|  |  |
| Q17. | In a cascaded mode, the number of vectored interrupts provided by 8259A is |
| Option A: | 4 |
| Option B: | 8 |
| Option C: | 16 |
| Option D: | 64 |
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| Q18. | GATE pin is used to control |
| Option A: | Paging |
| Option B: | Counting |
| Option C: | Instruction |
| Option D: | Data |
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| Q19. | the 80386DX has an address bus of |
| Option A: | 8 address lines |
| Option B: | 16 address lines |
| Option C: | 32 address lines |
| Option D: | 64 address lines |
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| Q20. | The operating frequency of 80386DX is |
| Option A: | 12 MHz and 20 MHz |
| Option B: | 20 MHz and 33 MHz |
| Option C: | 32 MHz and 12 MHz |
| Option D: | 30 MHz and 10 MHz |
|  |  |
| Q21. | The memory management unit consists of |
| Option A: | segmentation unit |
| Option B: | paging unit |
| Option C: | segmentation and paging units |
| Option D: | Memory block |
|  |  |
| Q22. | Pentium processor include branch prediction logic to |
| Option A: | To memory management |
| Option B: | To fetch instruction |
| Option C: | To minimize pipeline flushing |
| Option D: | To execute instruction |
|  |  |
| Q23. | The number of stages of the integer pipeline, U, of Pentium is |
| Option A: | 2 |
| Option B: | 4 |
| Option C: | 5 |
| Option D: | 6 |
|  |  |
| Q24. | To indicate that DMA transfer is about to begin which pin is used |
| Option A: | DMC |
| Option B: | DLD |
| Option C: | DRQ |
| Option D: | DACK |
|  |  |
| Q25. | The fifth stage of integer pipeline is also known as |
| Option A: | read back stage |
| Option B: | read forward stage |
| Option C: | write back stage |
| Option D: | Write forward stage |